Single-Mode 100GBASE-LR4
CFP2 Transceiver

Особенности:
- 103Gbps aggregate bit rates
- single 3.3V Power Supply
- Power dissipation < 12W
- Up to 10km transmission on SMF
- Hot-Pluggable CFP2 Footprint Duplex LC Connector Interface
- Compliant with CFP MSA Specification
- MDIO interface with integrated Digital Diagnostic Monitoring
- 4 x 25G electrical interface

Области применения:
- 100GBASE-LR4 Ethernet

Part No.	Data Rate	Fiber	Distance*(note1)	Interface	Temp.	DDMI
CFP2.100G.LR4	103Gbps	SMF	10km	LC	Standard	Yes

Note1: 10km with 9/125μm SMF

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	CFP2.100G.LR4	0		+70	°C
Power Supply Voltage	Vcc		3.2	3.3	3.4	V
Power Consumption	P				12	

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Input Amplitude (Differential)	Vin			1050	mVpp	AC coupled inputs*(Note7)
Input Impedance (Differential)	Zin	80	100	120	ohms	Rin > 100 kohms @ DC
Receiver						
Output Amplitude (Differential)	Vout	360		770	mVpp	AC coupled outputs*(Note7)
Output Impedance (Differential)	Zout	80	100	120	ohms	
Output Rise/Fall Time	t_r/t_f	24			ps	20%~80%

1.2V MDIO Interface Specifications

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Input Voltage	V_{IH}	0.84		1.5	V	
	V_{IL}	-0.3		0.36	V	
Input Leak current	I_{IN}	-100		100	uA	
Output Voltage	V_{OH}	1.0		1.5	V	
	V_{OL}	-0.3		0.2	V	
Input Capacitance	C_I			10	pF	
Input MDC Clock	f_{MDC}	0.1		4	MHz	
MDC Clock Period	T_{MDC}	250		10000	ns	
MDIO Hold Time	T_{hold}	10			ns	
MDIO SetupTime	T_{setup}	10			ns	
GLB_ALM	$T_{glb\_alm\_ass}$			150	ms	
	$T_{glb\_alm\_dea}$			150	ms	

Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		27.95		Gbps
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power*(Note5)	Po	-		**8.9**	dBm

Average Launch Power per Lane	Peach	**-2.5**		**2.9**	dBm
Side Mode Suppression Ratio	SMSR	30			dB
Optical Return Loss Tolerance				20	dB
Extinction Ratio*(Note6)	ER	7			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note6)		G.959.1 Compliant			
TX Disable Assert Time	t_off			100	us
Receiver					
Signaling Speed per Lane	BR_{AVE}		27.95		Gbps
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane*(Note8)	Rpow1	**-10.6**		4	dBm
Average Receive Power per Lane*(Note9)	Rpow	-8.8		2.9	dBm
Receive Sensitivity per Lane*(Note10)	Pmin1			**-10.6**	dBm
Receive Sensitivity per Lane*(Note11)	Pmin2			-10.3	dBm
Receiver Overload per Lane	Pmax	**4.5**			dBm
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-21			dBm
LOS De-Assert	LOSD			-11	dBm
LOS Hysteresis		0.5			dB

Note5: Output is coupled into a 9/125μm single-mode fiber.

Note6: Filtered, measured with a PRBS 2^{31}-1 test pattern @27.95Gbps

Note7: High speed I/O, internally AC coupled.

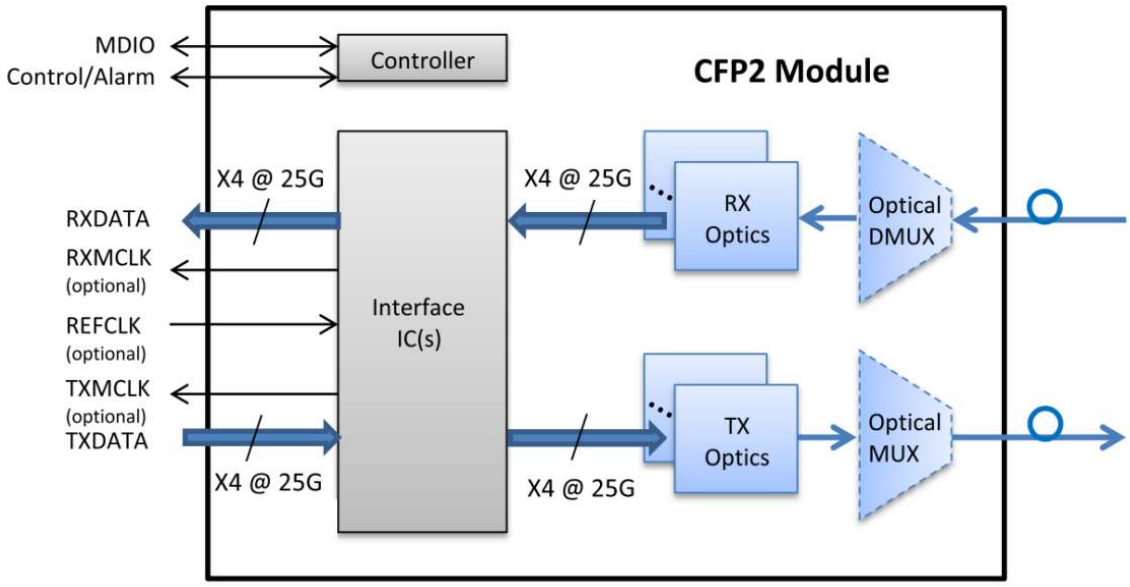
Note8: CFP transceiver works in 100GBASE-LR4 mode.

Note9: CFP transceiver works in OTU4 4I1-9D1F mode.

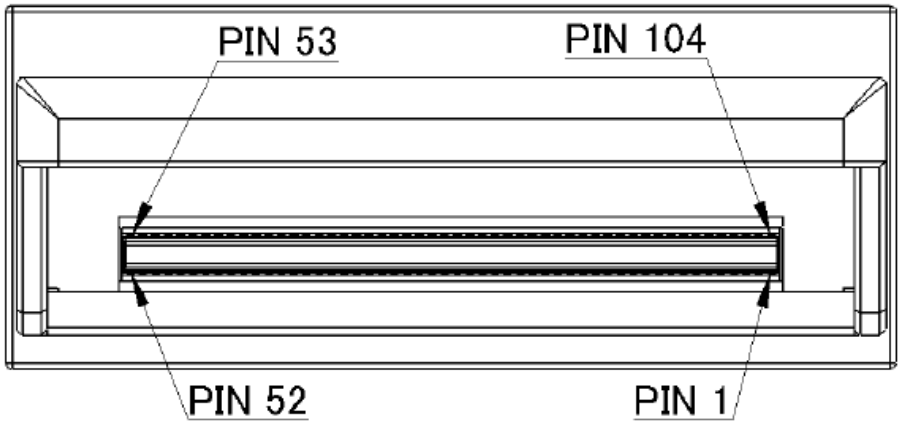
Note10: Minimum average optical power measured at BER less than 1E-12, with a 2^{31}-1 PRBS@25.78Gbps.

Note11: Minimum average optical power measured at BER less than 1E-12, with a 2^{31}-1 PRBS@27.95Gbps.

Functional Description of Transceiver



CFP2 Transceiver Electrical Pad Layout



Pin Function Definitions

CFP2	
Bottom	
1	GND
2	*(TX_MCK_N)*
3	*(TX_MCK_P)*
4	GND
5	N.C.
6	N.C.

CFP2	
Top	
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p

7	3.3V_GND
8	3.3V_GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V_GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V_GND

98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	*(REFCLKn)*
78	*(REFCLKp)*
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p

46	3.3V_GND
47	N.C.
48	N.C.
49	GND
50	*(RX_MCK_N)*
51	*(RX_MCK_P)*
52	GND

59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
53	GND

Bottom Row Pin Descriptions

Pin Num.	Name	Function	Notes
1	GND		
2	*(TX_MCK_N)*	O CML	For optical waveform testing. Not for normal use.
3	*(TX_MCK_P)*	O CML	For optical waveform testing. Not for normal use.
4	GND		
5	N.C.		
6	N.C.		
7	3.3V_GND		
8	3.3V_GND		
9	3.3V		3.3V Module Supply Voltage
10	3.3V		
11	3.3V		
12	3.3V		
13	3.3V_GND		
14	3.3V_GND		
15	VND_IO_A		Module Vendor I/O A. Do not connect!
16	VND_IO_B		Module Vendor I/O B. Do not connect!
17	PRG_CNTL 1		Programmable control 1 set over MDIO, MSA default: TRXIC_RSTn. TX&RX ICs reset. “0”: reset; “1” or NC: enabled = not used.
18	PRG_CNTL 2		Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used
19	PRG_CNTL 3		Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01": ≤6W, "10": ≤9W, "11" or NC: ≤12W = not used

20	PRG_ALRM 1		Programmable alarm 1 set over MDIO, MSA default: HIPWR_ON. “1”: module power up completed; “0”: module not high powered up.
21	PRG_ALRM 2		Programmable alarm 2 set over MDIO, MSA default: MOD_READY. “1”: ready; “0”: not ready.
22	PRG_ALRM 3		Programmable alarm 3 set over MDIO, MSA default: MOD_FAULT, fault detected. “1”: fault; “0”: not fault.
23	GND		
24	TX_DIS	I LVCMOS	Transmitter disable for all lanes. “1” or NC: transmitter disabled; “0”: transmitter enabled.
25	RX_LOS	O LVCMOS	Receiver loss of optical signal. “1”: low optical signal; “0”: normal condition.
26	MOD_LOPWR	I LVCMOS	Module Low power mode. “1” or NC: module in low power (safe) mode; “0”: power-on enabled.
27	MOD_ABS	O GND	Module Absent. “1”or NC: module absent; “0”: module present. Pull up resistor on Host.
28	MOD_RSTn	I LVCMOS	Module Reset. “0”: resets the module; “1” or NC: module enabled. Pull Down Resistor in module.
29	GLB_ALRMn	O LVCMOS	Global Alarm. “0”: alarm condition in any MDIO alarm register; “1”: no alarm condition. Open Drain, Pull up resistor on Host
30	GND		
31	MDC	I 1.2V CMOS	Management Data Clock
32	MDIO	I/O 1.2V CMOS	Management Data I/O bi-directional data
33	PRTADR0	I 1.2V CMOS	MDIO Physical Port address bit 0
34	PRTADR1	I 1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I 1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O	Module Vendor I/O C. Do not connect!
37	VND_IO_D	I/O	Module Vendor I/O D. Do not connect!
38	VND_IO_E	I/O	Module Vendor I/O E. Do not connect!
39	3.3V_GND		
40	3.3V_GND		
41	3.3V		3.3V Module Supply Voltage
42	3.3V		
43	3.3V		

44	3.3V		
45	3.3V_GND		
46	3.3V_GND		
47	N.C.		No Connect
48	N.C.		No Connect
49	GND		
50	*(RX_MCK_N)*	O CML	For optical waveform testing. Not for normal use.
51	*(RX_MCK_P)*	O CML	For optical waveform testing. Not for normal use.
52	GND		

Top Row Pin Descriptions

Pin Num.	Name	Function	Notes
53	GND		
54	N.C.		
55	N.C.		
56	GND		
57	RX0p	Lane 0 Rx Output O	CML Output
58	RX0n		
59	GND		
60	RX1p	Lane 1 Rx Output O	CML Output
61	RX1n		
62	GND		
63	N.C.		
64	N.C.		
65	GND		
66	N.C.		
67	N.C.		
68	GND		
69	RX2p	Lane 2 Rx Output O	CML Output
70	RX2n		
71	GND		
72	RX3p	Lane 3 Rx Output O	CML Output
73	RX3n		
74	GND		
75	N.C.		
76	N.C.		

77	GND		
78	*(REFCLKn)*	*Reference Clock I*	*Reference Clock Input*
79	*(REFCLKp)*		
80	GND		
81	N.C.		
82	N.C.		
83	GND		
84	TX0p	Lane 0 Tx Input I	CML Input
85	TX0n		
86	GND		
87	TX1p	Lane 1 Tx Input I	CML Input
88	TX1n		
89	GND		
90	N.C.		
91	N.C.		
92	GND		
93	N.C.		
94	N.C.		
95	GND		
96	TX2p	Lane 2 Tx Input I	CML Input
97	TX2n		
98	GND		
99	TX3p	Lane 3 Tx Input I	CML Input
100	TX3n		
101	GND		
102	N.C.		
103	N.C.		
104	GND		

Mechanical Specifications