OptiCin

Single-Mode 40GBASE-LR4 QSFP+ Transceiver

Особенности:
- соответствие стандарту IEEE 802.3ba (40GBASE-LR4)
- соответствие QSFP+ MSA SFF-8436 спецификации
- до 10км на одномодовом оптическом кабеле
- DFBs and PIN monitor photodiodes array for transmitter section
- PIN detectors and TIAs array for receiver section
- четыре 10Gbps CWDM канала в диапазоне 1300нм
- MDIO interface with integrated Digital Diagnostic Monitoring
- два стандартных LC оптических коннектора
- рабочая температура 0℃~+65℃

Области применения:
- 40GBASE-LR4 Ethernet links
- InfinitiBand QDR and DDR interconnects Client-side
- 40G Telecom connections

Part No.	Data Rate	Fiber	Distance*(note1)	Interface	Temp.	DDMI
QSFP-Plus-LR	40Gbps	SMF	10km	LC	-0℃~+65℃	Yes

Note1: Over SMF

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_A	QSFP-Plus-LR	0		+70	°C
Power Supply Voltage	Vcc		3.15	3.3	3.45	V
Power Supply Current	Icc				1100	mA
Aggregate Bit Rate	BR_{AVE}			41.25		Gbps
Lane Bit Rate	BR_{LANE}			10.3125		Gbps

Performance Specifications - Electrical

Parameter		Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter							
Single ended input voltage tolerance			-0.3		4	V	Referred to TP1 signal common
AC common mode input voltage tolerance			15			mV	RMS
Input Impedance (Differential)		Zin	85	100	115	ohms	Rin > 100 kohms @ DC
TX Disable	Disable	V_{IH}	2		Vcc+0.3	V	
	Enable	V_{IL}	0		0.8		
TX FAULT	Fault	V_{OH}	2.4		Vcc+0.3	V	
	Normal	V_{OL}	0		0.5		
Receiver							
Single ended output voltage			-0.3		4	V	Referred to signal common
AC common mode voltage					7.5	mV	RMS
Termination mismatch at 1MHz					5	%	
Output Impedance (Differential)		Zout	85	100	115	ohms	
Output Rise/Fall Time		t_r/t_f	30			ps	10%~90%
RX_LOS	LOS	V_{OH}	2.4		Vcc+0.3	V	
	Normal	V_{OL}	0		0.8	V	

Optical and Electrical Characteristics

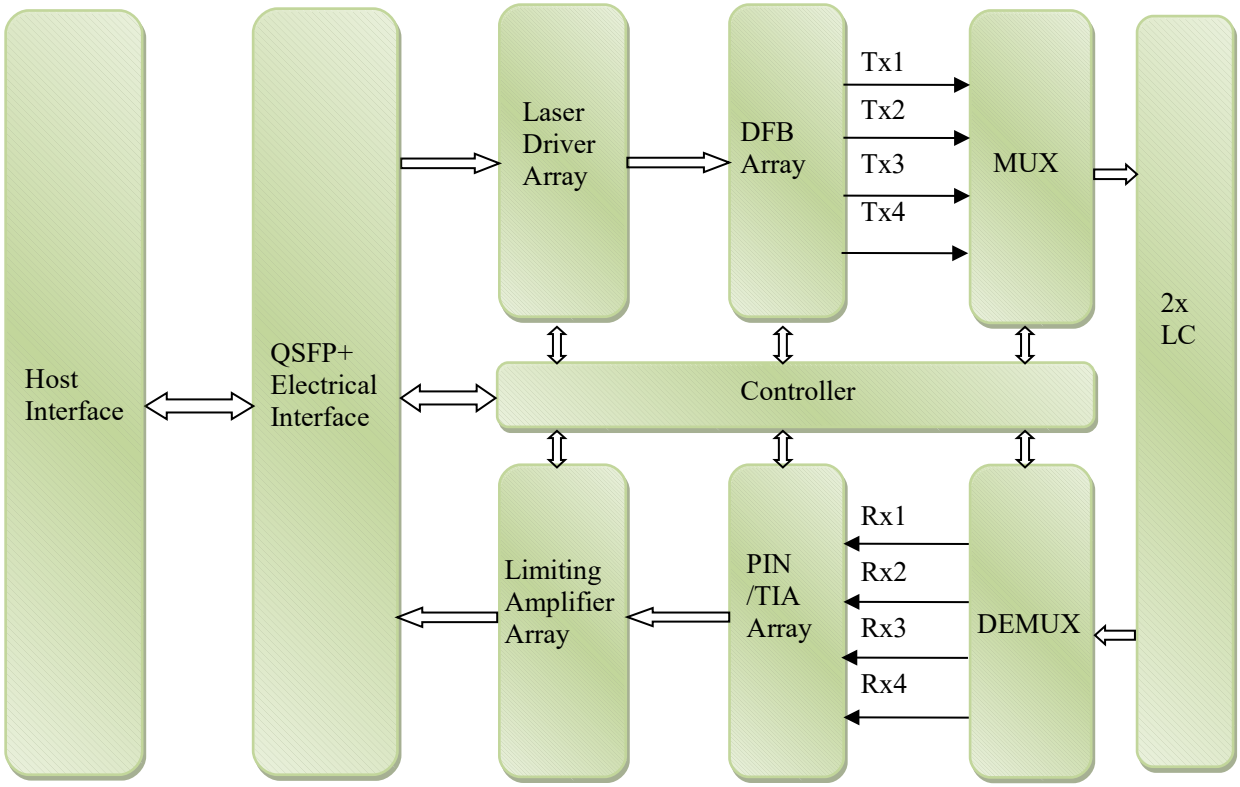
Parameter	Symbol	Min.	Typical	Max.	Unit
SMF	L	-	10	-	km
Aggregate Bit Rate	BR_{AVE}	-	40	-	Gbps
Per Lane Bit Rate	BR_{LANE}	-	10.3125	-	Gbps
Transmitter					
Channels wavelength	λ_C	-	1271	-	nm
		-	1291	-	
		-	1311	-	
		-	1331	-	
-20dB spectral width	$\Delta\lambda$	-	-	1	nm
Average Launch Power, Each Lane*(note2)	Pout/lane	**-4**	-	2	dBm
Transmit OMA, per Lane	TX_OMA/lane	-4	-	3.5	dBm
Extinction Ratio	Er	3	3.5	-	dB
Output Optical Eye*(note3)	IEEE 802.3ba-2010 Compliant				
Receiver					
Channels wavelength	λ_C	-	1271	-	nm
		-	1291	-	
		-	1311	-	

		-	1331	-	
Damage Threshold		3	-	-	dB
Stressed receiver sensitivity in OMA, each lane	Pmins	**-11.5**	-	-13	dBm
Maximum Receive Power, each lane	Pmax	-	-	**2.4**	dBm
Receiver reflectance	Rr	-	-	-12	dB

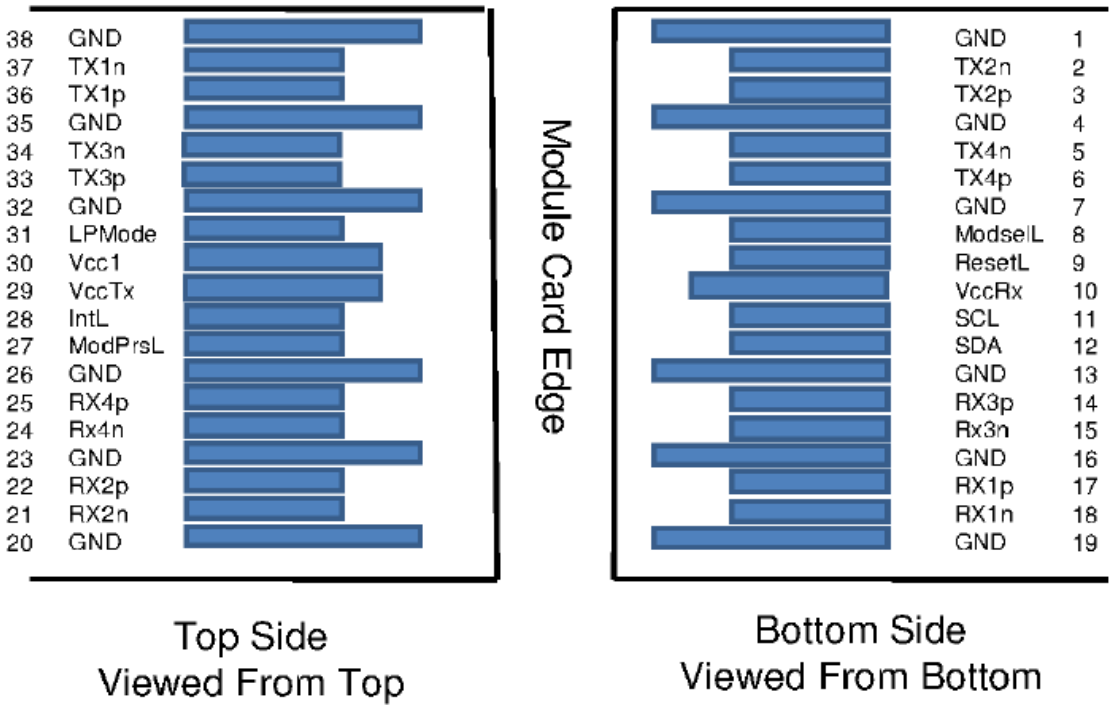
Note2: Output is coupled into a 9/125μm Single-Mode fiber.

Note3: Filtered, measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps

Functional Description of Transceiver



QSFP+ Transceiver Electrical Pad Layout



Pin Arrangement and Definition

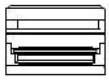
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	

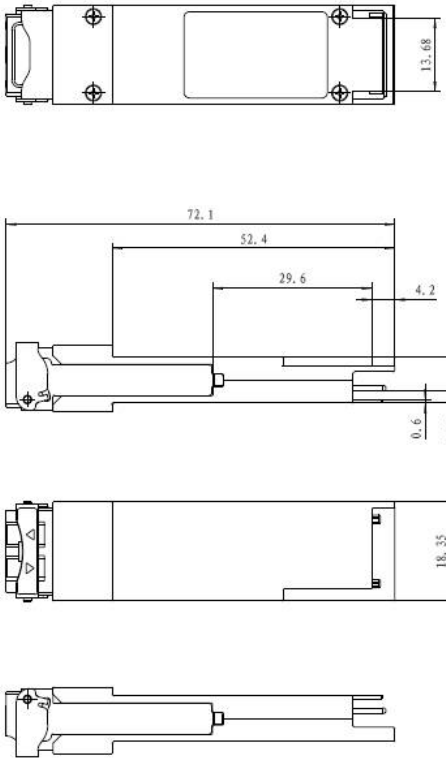
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500mA.

Mechanical Specifications

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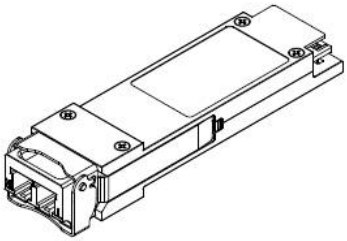
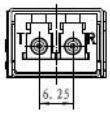
29.6
4.2
8.5
0.6
2.25
18.35

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