XFP модуль. Модель **XFP-SR.LC.03**

Особенности:

- 850нм лазер
- возможность горячей замены
- двойной LC разъем
- встроенная функция диагностики
- мощность рассеивания < 3,5Вт
- температурный диапазон от -5 до +70°C
- соответствие спецификации XFP MSA Rev 4.5

Области применения:

– 10GBASE-SR 10G Ethernet

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T_A	SFP-Plus-SR.LC.03	-5		+70	°C
Power Supply Voltage	V_{CC}		3.15	3.3	3.45	V
Power Supply Current	I_{CC}				300	mA
Surge Current	I_{Surge}				+30	mA
Baud Rate				10.3125	10.5	GBaud

PERFORMANCE SPECIFICATIONS - ELECTRICAL

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
TRANSMITTER						
CML Inputs(Differential)	Vin	150		1200	mVp	AC coupled inputs
Input Impedance (Differential)	Zin	85	100	115	ohms	Rin > 100 kohms @ DC
Tx_DISABLE Input Voltage - High		2		3.45	V	
Tx_DISABLE Input Voltage - Low		0		0.8	V	
Tx_FAULT Output Voltage -- High		2		Vcc+0.3	V	Io = 400µA; Host Vcc

Tx_FAULT Output Voltage -- Low		0		0.5	V	Io = -4.0mA
RECEIVER						
CML Outputs (Differential)	Vout	350		700	mVpp	AC coupled outputs
Output Impedance (Differential)	Zout	85	100	115	ohms	
Rx_LOS Output Voltage - High		2		Vcc+0.3	V	Io = 400µA; Host Vcc
Rx_LOS Output Voltage - Low		0		0.8	V	Io = -4.0mA
MOD_DEF (0:2)	VoH	2.5			V	With Serial ID
	VoL	0		0.5	V	

Optical and Electrical Characteristics

Parameter		Symbol	Min.	Typical	Max.	Unit
50/125 MMF				300		m
Data Rate				10.3		Gbps
Transmitter						
Centre Wavelength		λ_C	840	850	860	nm
Spectral Width (RMS)		σ			0.45	nm
Average Output Power		P_{0ut}	-7.3		-1	dBm
Transmitter Dispersion Penalty		TDP			3.9	dB
Input Differential Impedance		Z_{IN}	90	100	110	Ω
TX Disable	Disable		2.0		Vcc+0.3	V
	Enable		0		0.8	
TX_Fault	Fault		2.0		V_{CC}+0.3	V
	Normal		0		0.8	
TX_Disable Assert Time		t_off			10	us
Receiver						
Centre Wavelength		λ_C	840	850	860	nm
Receiver Sensitivity		PIN			-13.3	dBm
Output Differential Impedance		P_{IN}	90	100	110	Ω
Receiver Overload		P_{MAX}	-1			dBm
Optical Return Loss		ORL			-12	dB
LOS De-Assert		LOS_D			-15	dBm
LOS Assert		LOS_A	-25			dBm
LOS	High		2.0		V_{CC}+0.3	V
	Low		0		0.8	

Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1

2		VEE5	Optional –5.2 Power Supply – Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to , respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready;	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

3. A Reference Clock input is not required .

Hostboard Connector Pinout

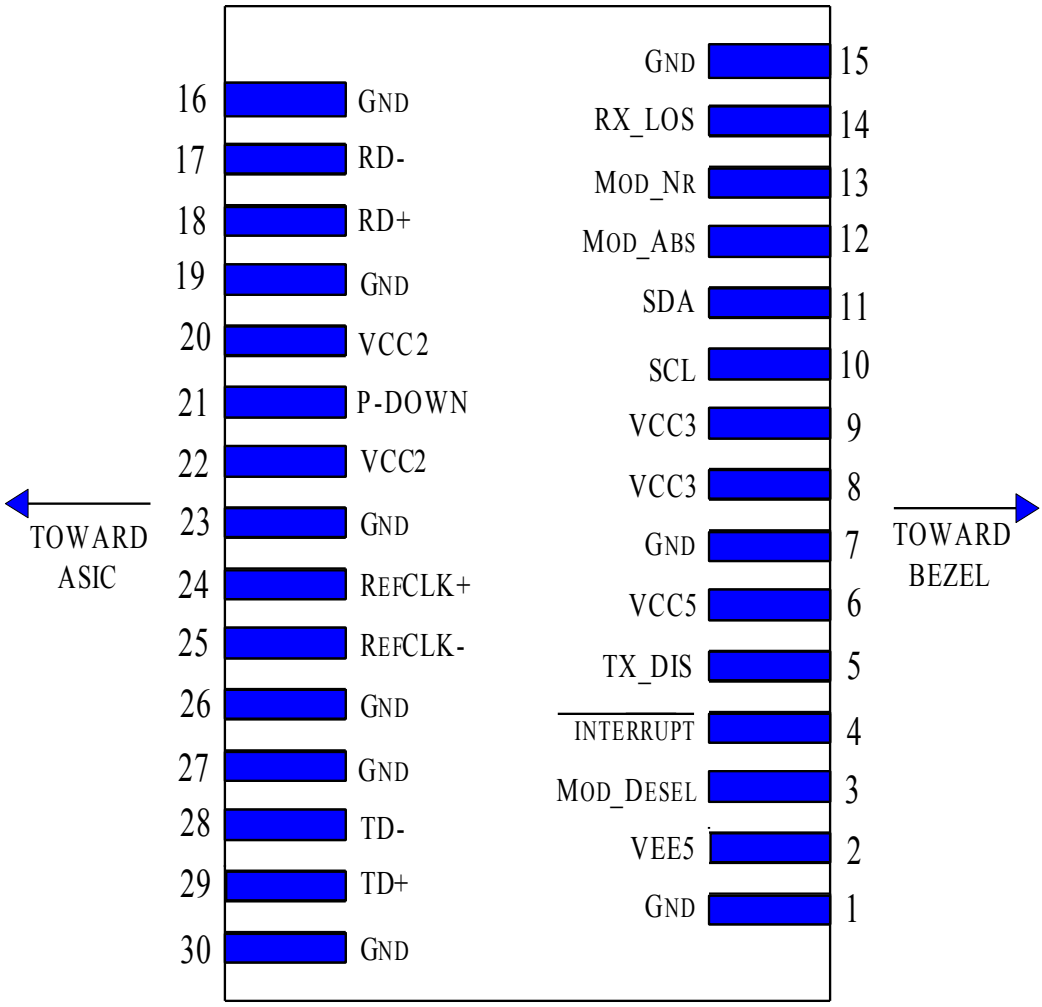


Diagram of Host Board Connector Block Pin Numbers and Name

General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	9.95		11.1	Gb/s	1
Bit Error Ratio	BER			10^{-12}		2
Max. Supported Link Length	LMAX		10		km	1

Notes:

1. 10GBASE-LR/LW, 1200-SM-LL-L
2. Tested with a $2^7 – 1$ PRBS

Digital Diagnostic Functions

XFP-LR.LC.10 Small Form Factor 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification Rev 4.5.

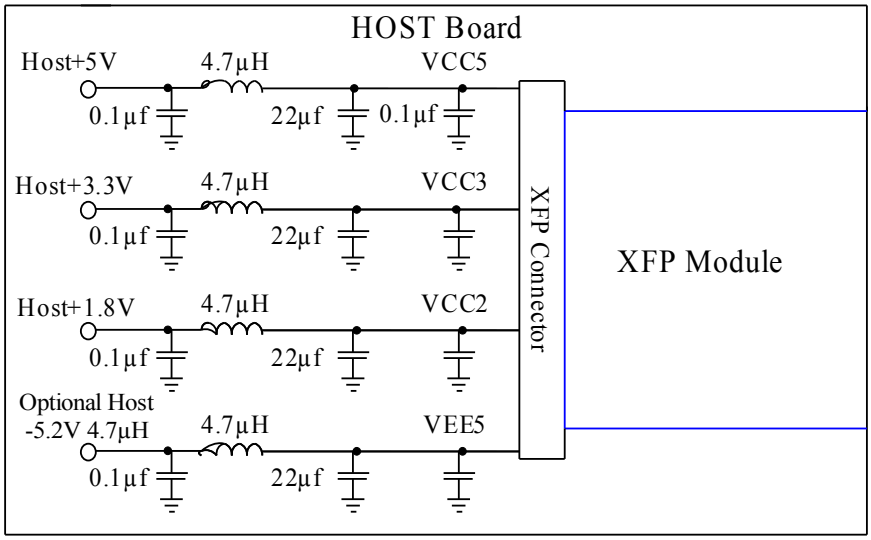
As defined by the XFP MSA, XFP-LR.LC.10 XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- . Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

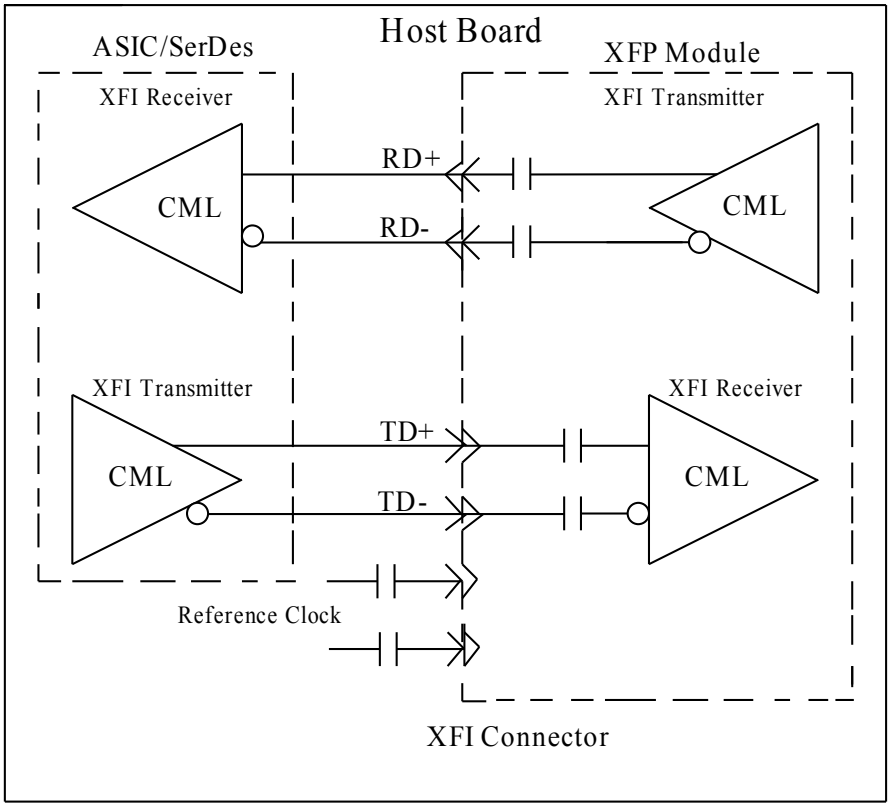
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

Recommended Host Board Power Supply Circuit



Recommended High-speed Interface Circuit



Mechanical Specifications

XFP-LR.LC.10 XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).