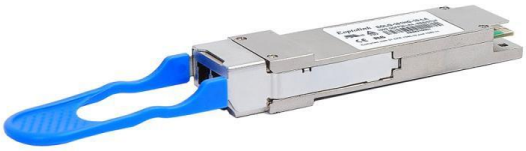
QSFP28.100G.ER4

QSFP28, 100G, ER4, 40km, 2xLC



Особенности:

- 103Gbps
- одно питание 3.3V, Power dissipation < 4.5W
- до 40км на одномодовом оптическом кабеле (SMF)
- 4 по 25Gbps EML LAN-WDM канала со стороны передатчика
- APD и TIA array фотоприемники
- 4x25G электрический интерфейс
- дуплексный LC коннектор
- I2C интерфейс с диагностикой (Digital Diagnostic Monitoring)

Области применения:

- 100GBASE-ER4 100G Ethernet

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
QSFP28.100G.ER4*(note1)	103Gbps	SMF	40km	LC	0℃~+70℃	Yes

Note1: also support 103Gbps

Note2: Over SMF

*The product image only for reference purpose.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_c	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	P_D			5	W

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Transmitter						
Differential Input amplitude				900	mv_{p-p}	
Input Impedance (Differential)	Zin			10	%	
Stressed input parameters						
Eye width		0.46			UI	
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13				
Eye height		95			mv	
DC common mode voltage		-350		2850	mv	
Receiver						
Differential output amplitude		200		900	mvp-p	
Output Impedance (Differential)	Zout			10	%	
Eye width		0.57			UI	
Eye height differential		228			mv	
Vertical eye closure				5.5	dB	

Optical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Total Average Output Power*(Note3)	Po			8.9	dBm

Average Launch Power per Lane	Peach	-2.5		2.9	dBm
Average launch power of OFF transmitter per lane				-30	dBm
Side-mode suppression ratio	$SMSR_{min}$	30			dB
Difference in launch power between any two lanes (OMA)				4	dB
Optical Return Loss Tolerance		20			dB
Transmitter reflectance*(Note5)				-26	
Extinction Ratio*(Note6)	ER	8			dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note6)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Receiver					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data Rate Variation		-100		+100	ppm
Damage threshold	Rdam	-3			dBm
Lane_0 Center Wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average Receive Power per Lane*(Note7)	Rxpow	-20.5		-3.5	dBm
Receive Sensitivity in OMA per Lane*(Note8)	Rxsens			-18.5	dBm
Stressed Receiver Sensitivity (OMA) per Lane*(Note9)	RX_{SRS}			-16	dBm
Optical Return Loss	ORL			-26	dB
LOS Assert	LOSA	-35			dBm
LOS De-Assert	LOSD			-25	dBm
LOS Hysteresis		0.5			dB
Conditions of stressed receiver sensitivity test:					
Vertical eye closure penalty*(Note10)	VECP		dB		
Stressed eye J2 Jitter*(Note10)	J2		UI		
Stressed eye J4 Jitter*(Note10)	J4		UI		

SRS eye mask defination {X1, X2, X3, Y1, Y2, Y3}*(Note10)		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}	

Note3: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note4: Even if the TDP < 1.0dB, the OMA (min) must exceed this value. Note5: Transmitter reflectance is defined looking into the transmitter.

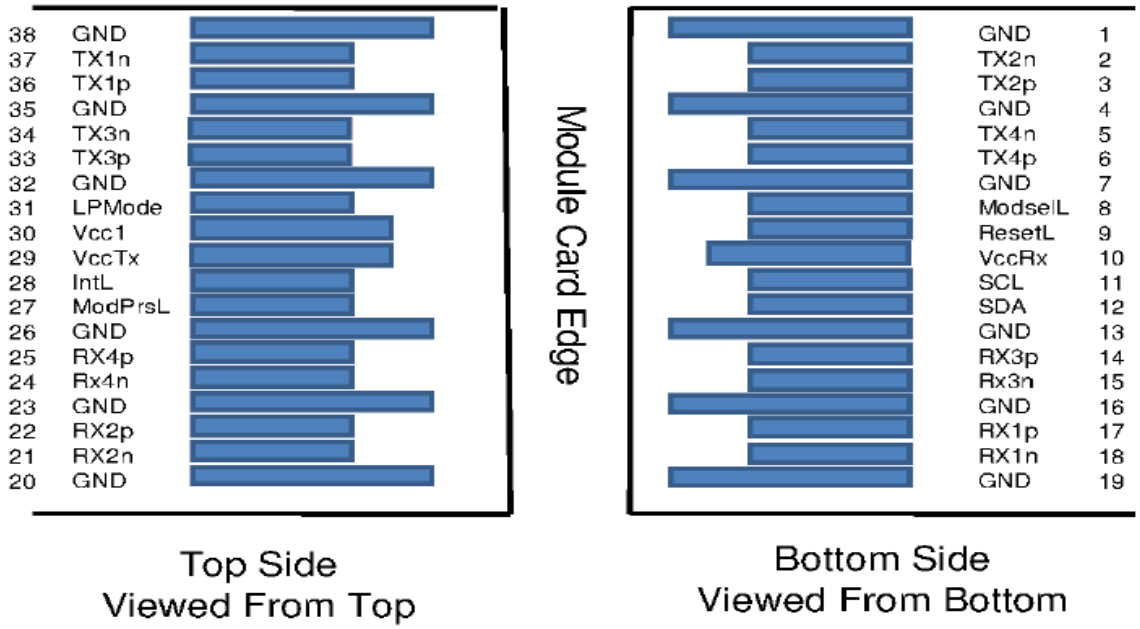
Note6: Eye mask hit ratio is 5E-5.

Note7: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance. Note8: Receiver sensitivity (OMA), each lane (max) at 5E-5 BER is a normative specification.

Note9: Measured with conformance test signal at TP3 for BER = 5*10-5.

Note10: Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

QSFP28 Transceiver Electrical Pad Layout



Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are					

common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 500mA.

Mechanical Specifications

